REMARKS

Claims 1 through 9 are currently pending in the application.

This amendment is in response to the Office Action of November 15, 2002.

Supplemental Information Disclosure Statement

Applicants note the filing of a Supplemental Information Disclosure Statement herein on March 1, 2002, and note that no copy of the PTO-1449 was returned with the outstanding Office Action. Applicant respectfully requests that the information cited on the PTO-1449 be made of record herein.

Amendment in Response to Office Action of May 8, 2002

Applicant's undersigned attorney notes the filing herein of an Amendment on August 7, 2002, which filing was not acknowledged in the outstanding Office Action. Should the Amendment have failed for some reason to have been entered in the Office file, Applicant's undersigned attorney will be happy to have a true copy thereof hand-delivered to the Examiner.

35 U.S.C. § 103(a) Obviousness Rejections

Claims 1 and 6 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Schneider et al. (U.S. Patent 5,610,442) in combination with MacDonald, Jr. et al. (U.S. Patent 5,905,638).

Claims 3 through 5, 8 and 9 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Chiu et al. (U.S. Patent 6,121,680) in combination with MacDonald, Jr. et al. (U.S. Patent 5,905,638).

Applicant further submits that to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited prior art reference must teach or suggest all of the claim limitations. Furthermore, the suggestion to make the claimed

combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicant's disclosure.

Applicant submits that any combination of the Schneider et al. reference in combination with MacDonald, Jr. et al reference cannot establish a prima facie case of obviousness under 35 U.S.C. § 103 regarding the presently claimed invention of amended independent claims 1 and 6 of the present application because, at the very least, the combination of the cited prior art does not teach or suggest all the claim limitations of the presently claimed invention. For instance, no combination of the cited prior art teaches or suggests the claim limitations of the presently claimed invention of amended claims 1 and 6 calling for "a layer of adhesive substantially covering a surface of the gel elastomer" and "a heat sink attached to the gel elastomer by the layer of adhesive". Neither the Schneider et al. reference nor the MacDonald, Jr. et al. reference, nor any combination thereof teaches or suggests a layer of adhesive as set forth in the presently claimed invention. Accordingly, the cited prior art cannot and does not establish a prima facie case of obviousness under 35 US.C. § 103 regarding the presently claimed invention of amended independent claims 1 and 6. Therefore, independent claims 1 and 6 are allowable as well as dependent claims 2 and 7 therefrom.

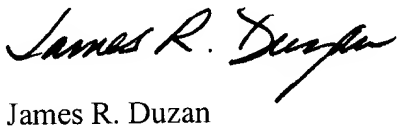
Similarly, Applicant submits that the cited prior art combination of Chiu et al reference in combination with MacDonald, Jr. et al reference cannot establish a prima facie case of obviousness under 35 U.S.C. § 103 regarding the presently claimed invention of amended independent claims 3 and 8 of the present application because, at the very least, the combination of the cited prior art does not teach or suggest all the claim limitations of the presently claimed invention. For instance, no combination of the cited prior art teaches or suggests the claim limitations of the presently claimed invention of amended claims 3 and 8 calling for "one of a glob top material and low viscosity polymeric material filing any space between the substrate and the semiconductor die". Neither the Chiu et al reference, nor the MacDonald, Jr. et al. reference, not any combination of the Chiu et al reference and the MacDonald, Jr. et al reference teaches or suggests any such claim limitations whatsoever. Accordingly, the cited prior art cannot and does not establish a prima facie case of obviousness under 35 US.C. § 103 regarding the presently

claimed invention of amended independent claims 3 and 8. Therefore, claims 3 and 8 are allowable as well as dependent claims 4, 5, and 9 therefrom.

In summary, Applicant submits that claims 1 through 9 are clearly allowable over the cited prior art.

Applicants request the allowance of claims 1-9 and the case passed for issue.

Respectfully submitted,



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Enclosure: Version with Markings to Show Changes Made

Document in ProLaw

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

A marked-up version of paragraph **[0001]**, highlighting the changes thereto, follows:

[0001] Cross Reference to Related Applications: This application is a continuation of application Serial No. 09/510,894, filed February 23, 2000, [pending] now U.S. Patent 6,229,204 B1, issued May 8, 2001, which is a divisional of application Serial No. 09/146,945, filed September 3, 1998, now U.S. Patent 6,117,797, issued September 12, 2000.

IN THE CLAIMS:

A marked-up version of each of the presently amended claims, highlighting the changes thereto, follows:

1. (Four Times Amended) A semiconductor assembly comprising:

a substrate having a surface;

a semiconductor die having a plurality of edges, having an active surface having a plurality of bond pads thereon located adjacent at least two edges of the plurality of edges, and having a back side surface, the semiconductor die having at least a portion of the back side surface adhesively attached to at least a portion of the surface of the substrate;

a gel elastomer contacting at least a portion of the active surface of the semiconductor die;

a layer of adhesive substantially covering a surface of the gel elastomer;

a heat sink attached to the gel elastomer by the layer of adhesive; and

an encapsulation material covering a portion of the surface of the substrate, the plurality of edges of the semiconductor die, and at least one bond pad of the plurality of bond pads located adjacent at least two edges of the semiconductor die, wherein the encapsulation material excludes covering the heat sink.

3. (Twice Amended) A semiconductor assembly comprising:

a substrate having a plurality of circuits on a portion of a surface thereof;

a semiconductor die having a plurality of bond pads located on an active surface thereof and having a back side surface;

a plurality of solder balls connecting at least a portion of the plurality of bond pads of the semiconductor die to at least a portion of the plurality of circuits of the substrate;

one of a glob top material and low viscosity polymeric material filing any space between the substrate and the semiconductor die;

a gel elastomer contacting at least a portion of the back side surface of the semiconductor die, wherein the gel elastomer is compliant, adhesive, and filled with a thermally conductive material; and

a heat sink cap covering the gel elastomer, the semiconductor die, the plurality of solder balls, and a portion of the substrate, the heat sink cap contacting at least a portion of the gel elastomer.

6. (Four Times Amended) A semiconductor assembly comprising:

a substrate having a plurality of electrical connections on a portion of a surface thereof;

at least one semiconductor die having a plurality of bond pads on a first portion of an active surface thereof and having a back side surface, a portion of the back side surface adhesively attached to a portion of the surface of the substrate;

a plurality of wire bonds connecting at least a portion of the plurality of bond pads of the at least one semiconductor die to at least a portion of the plurality of electrical connections of the substrate;

a layer of adhesive substantially covering a surface of the gel elastomer

a gel elastomer contacting a second portion of the active surface of the at least one semiconductor die;

a heat sink attached to the gel elastomer by the layer of adhesive; and

an encapsulant material covering a portion of the surface of the substrate, the plurality of bond pads on the active surface of the at least one semiconductor die, a portion of the active surface of the at least one semiconductor die, and the plurality of wire bonds, wherein the encapsulation material excludes covering the heat sink.

8. (Three Times Amended) A semiconductor assembly comprising:

a substrate having a surface having a plurality of circuits on a portion thereof;

a semiconductor die having a plurality of bond pads located on a first portion of an active surface thereof and having a back side surface;

a plurality of solder balls connecting at least a portion of the plurality of bond pads of the semiconductor die to at least a portion of the plurality of circuits of the substrate;

one of a glob top material and low viscosity polymeric material filing any space between the substrate and the semiconductor die;

a gel elastomer contacting a portion of the back side surface of the semiconductor die, wherein the gel elastomer is a cross-linked silicon gel, compliant, adhesive, and filled with a thermally conductive material; and

a heat sink cap having a portion thereof in contact with a portion of the gel elastomer, the heat sink cap covering the gel elastomer, the semiconductor die, the plurality of solder balls, and at least a portion of the substrate.